Terms used **ovsf codes order bit** Found **72,503** of **198,617**

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1 Poster session 2: Orthogonal code generator for 3G wireless transceivers
Boris D. Andreev, Edward L. Titlebaum, Eby G. Friedman
April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI GLSVLSI '03**
Publisher: ACM Press
Full text available: pdf(152.16 KB) Additional Information: full citation, abstract, references, index terms

Orthogonal variable spreading factor (OVSF) codes are standard in third generation UMTS cellular systems. The efficient generation of these codes is essential for reducing the area and power of wireless transceivers. In this paper, the basic properties of this family of codes are analyzed from an RTL perspective and two efficient hardware code generators are proposed. Tradeoffs and design solutions as well as low power considerations are discussed. These results represent the first reported impl ...

Keywords: 3GPP, CDMA, OVSF codes, UMTS, VLSI, WCDMA

2 W1-C: general symposium: New non-blocking EOVSF codes for multi-rate WCDMA system
Yih-Fuh Wang, Hsing-Hu Chen, Tun-Ying Lin
July 2006 **Proceeding of the 2006 international conference on Communications and mobile computing IWCMC '06**
Publisher: ACM Press
Full text available: pdf(886.94 KB) Additional Information: full citation, abstract, references, index terms

Orthogonal variable spreading factor (OVSF) codes are employed in the third generation (3G) wideband code division multiple access (WCDMA) wireless system as channelization codes. Any two codes OVSF of different levels are orthogonal if and only if one of two codes is not ancestor/descendant in each other. Therefore, when an OVSF code is assigned to a user, it blocks all of its ancestor and descendant codes. This results in a major drawback of OVSF codes, called blocking property: When an OVSF c ...

Keywords: EOVSF codes, OVSF codes, WCDMA, third generation (3G)

3 Ad hoc networks: OVSF-CDMA code assignment in wireless ad hoc networks
Peng-Jun Wan, Xiang-Yang Li, Ophir Frieder
October 2004 **Proceedings of the 2004 joint workshop on Foundations of mobile computing DIALM-POMC '04**

Publisher: ACM Press

Full text available: pdf(198.79 KB) Additional Information: full citation, abstract, references, citings, index terms

Orthogonal Variable Spreading Factor (OVSF) CDMA code provides a means of support of variable rate data service at low hardware cost. In contrast to the conventional orthogonal fixed-spreading-factor CDMA code, OVSF-CDMA code consists of an infinite number of codewords with variable rates but not every pair of codewords are orthogonal to each other. In an OVSF-CDMA wireless ad hoc network, a code assignment has to be conflict-free, i.e., two nodes can be assigned the same codeword or two non-ort ...

Keywords: OVSF-CDMA, approximation algorithms, code assignment, graph theory, system design

4 Region division assignment: a new OVSF code reservation and assignment scheme for downlink capacity in W-CDMA systems

Rujipun Assarut, Ken'ichi Kawanishi, Ushio Yamamoto, Yoshikuni Onozato

May 2006 **Wireless Networks**, Volume 12 Issue 3

Publisher: Kluwer Academic Publishers

Full text available: pdf(3.18 MB) Additional Information: full citation, abstract, references, index terms

This work focuses on the efficient management of orthogonal-variable-spreading-factor (OVSF) codes for multimedia communications in the W-CDMA systems. Because these systems must assign only OVSF codes that are mutually orthogonal, even if they have sufficient transmission capacity they block connections for which no orthogonal OVSF codes are available. This code blocking can, with extra overhead, be eliminated by reassigning codes, but in this paper we propose an OVSF code management scheme des ...

Keywords: OVSF, W-CDMA, code assignment, code blocking

5 Closed-loop architecture and protocols for rapid dynamic spreading gain adaptation in CDMA networks

Lih-feng Tsaur, Daniel C. Lee

August 2006 **IEEE/ACM Transactions on Networking (TON)**, Volume 14 Issue 4

Publisher: IEEE Press

Full text available: pdf(928.82 KB) Additional Information: full citation, abstract, references, index terms

We present a closed-loop architecture and protocols for rapid dynamic spreading gain adaptation and fast feedback between a transmitter and a receiver communicating with each other in CDMA networks. These protocols and architecture do not require the transfer of an explicit control message indicating the change of CDMA spreading gain from transmitter to receiver. Also, with these protocols, the transmitter can change the spreading gain symbol-by-symbol as opposed to frame-by-frame, and feedback ...

Keywords: CDMA, OVSF codes, rate adaptation

6 An innovative simulation tool for advanced signal processing in UMTS systems

Dania Marabissi, Marco Michelini, Luca Simone Ronga

September 2004 **Wireless Networks**, Volume 10 Issue 5

Publisher: Kluwer Academic Publishers

Full text available: pdf(545.12 KB) Additional Information: full citation, abstract, references, index terms

Link-level simulations are essential in the design of UMTS communication systems. The

large number of interdependent variables makes it impossible to derive easy design steps without an efficient modeling of the environments and the implemented reception schemes. In this paper, a novel tool for UMTS design is presented. The tool includes a fast C++ simulation engine and a complete 3GPP library to model the uplink transmission chain. As an example, a series of Monte Carlo performance simulatio ...

Keywords: 3G-simulation environment, CDMA advanced receivers, DSP system design, code division multiple access (CDMA), fading channel models, multirate systems, object-oriented simulation tool

7 W1-C: general symposium: A multi-rate CDMA system with block-spreading schemes for anti-interference and high frequency efficiency

Mitsuhiro Tomita, Noriyoshi Kuroyanagi, Kohei Ohtake, Naoki Suehiro, Sinya Matsufuji

July 2006 **Proceeding of the 2006 international conference on Communications and mobile computing IWCMC '06**

Publisher: ACM Press

Full text available: pdf(342.74 KB) Additional Information: full citation, abstract, references, index terms

For mobile systems higher than 3G, multi-rate data service is becoming an important issue. This paper proposes a multi-rate block-spreading CDMA system as an efficient scheme which is capable of intra-cell-interference free operation and inter-cell-interference reduction by a factor of reciprocal of the spreading factor. With a use of an accurate pilot transmission scheme, it is shown that a high frequency utilization efficiency can be achieved for various mixed data rate services.

8 Power control based QoS provisioning for multimedia in W-CDMA

Özgür Gürbüz, Henry Owen

January 2002 **Wireless Networks**, Volume 8 Issue 1

Publisher: Kluwer Academic Publishers

Full text available: pdf(247.47 KB) Additional Information: full citation, abstract, references, index terms

Third generation wireless communication systems will support multimedia, and W-CDMA will be the common air interface technology. Due to the interference limited nature of CDMA, power is the main resource of the network, and power control is a means of resource management. In this article, we introduce Dynamic Resource Scheduling (DRS) as a framework which employs power control for QoS provisioning of multimedia traffic in W-CDMA. In DRS, we propose the application of optimal power assignment to ...

Keywords: WCDMA, power control, wireless QoS

9 Tools and Methodologies: Simulation tools for advanced signal processing in UMTS systems

Dania Marabissi, Marco Michelini, Luca Simone Ronga

September 2002 **Proceedings of the 5th ACM international workshop on Modeling analysis and simulation of wireless and mobile systems MSWiM '02**

Publisher: ACM Press

Full text available: pdf(317.64 KB) Additional Information: full citation, abstract, references, index terms

Link-level simulations are essential in the design of UMTS communication systems. The large number of inter-dependent variables makes it impossible to derive easy design steps without an efficient modeling of the environments and the implemented reception schemes. In this paper, a novel tool for UMTS design is presented. The tool includes a fast C++ simulation engine and a complete 3GPP library to model the uplink transmission chain. As an example, a series of Monte Carlo performance simulations ...

Keywords: 3G-simulation environment, CDMA advanced receivers, DSP system design, code division multiple access (CDMA), fading channel models, multirate systems, object oriented simulation tool

10 Standards: Proposed american standard: bit sequencing of the american standard code for information interchange (ACSII) in serial-by-bit data transmission

S. Gorn, R. W. Bemer, J. Green, E. Lohse
June 1964 **Communications of the ACM**, Volume 7 Issue 6
Publisher: ACM Press
Full text available: pdf(610.39 KB) Additional Information: full citation

11 M1-A: communication and information theory symposium: Performance analysis of multi chip/data rate DS-CDMA signals over multipath Rayleigh fading channels

Ertan Öztürk
July 2006 **Proceeding of the 2006 international conference on Communications and mobile computing IWCMC '06**
Publisher: ACM Press
Full text available: pdf(392.30 KB) Additional Information: full citation, abstract, references, index terms

This paper investigates the Probability error (P_e) performance of Multi-Chip/Data Rate Direct Sequence Code Divisions Multiple Access (MCDR/DS-CDMA) systems over multi-path Rayleigh fading channels. Two chip waveforms, raised cosine (RC) and an orthogonal wavelet, are compared numerically in terms of the Pe. The results represent that the wavelet based system significantly outperforms the RC based system in terms of the P_e•. On the other hand, the wavelets have greate ...

Keywords: chip waveforms, multi-chip/data rate CDMA, multipath fading channels, performance analysis, wavelets

12 Correspondences of 8-bit and Hollerith codes for computer environments—a USASI tutorial

E. Lohse
November 1968 **Communications of the ACM**, Volume 11 Issue 11
Publisher: ACM Press
Full text available: pdf(709.73 KB) Additional Information: full citation, abstract

The correspondence tables in the document reflect USASCII standard code assignments as well as other codes. Comments that refer to the assignments of characters or character sets in columns 8 through 15 of Table 1 as a basis for standardization are solicited.

Keywords: USA standard, card code, hole-patterns, hole-patterns assignment, punched card, punched card code, punched card systems

13 Native code compilation of Erlang's bit syntax

Per Gustafsson, Konstantinos Sagonas
October 2002 **Proceedings of the 2002 ACM SIGPLAN workshop on Erlang ERLANG '02**
Publisher: ACM Press
Full text available: pdf(196.81 KB) Additional Information: full citation, abstract, references, citings

Erlang's bit syntax caters for flexible pattern matching on bit streams (objects known as

binaries). Binaries are nowadays heavily used in typical Erlang applications such as protocol programming, which in turn has created a need for efficient support of the basic operations on binaries.To this effect, we describe a scheme for efficient native code compilation of Erlang's bit syntax. The scheme relies on *partial translation* for avoiding code explosion, an ...

14 Enhancing the performance of 16-bit code using augmenting instructions

Arvind Krishnaswamy, Rajiv Gupta

June 2003 **ACM SIGPLAN Notices , Proceedings of the 2003 ACM SIGPLAN conference on Language, compiler, and tool for embedded systems LCTES '03**, Volume 38 Issue 7

Publisher: ACM Press

Full text available: pdf(276.13 KB) Additional Information: full citation, abstract, references, citings, index terms

In the embedded domain, memory usage and energy consumption are critical constraints. Dual width instruction set embedded processors such as the ARM provide a 16-bit instruction set in addition to the 32-bit instruction set to address these concerns. Using 16-bit instructions one can achieve code size reduction and I-cache energy savings at the cost of performance. We have observed that throughout 16-bit Thumb code there exist Thumb instruction pairs that are equivalent to a single ARM instructi ...

Keywords: 16-bit thumb ISA, 32-bit ARM ISA, AX instructions, code size, embedded processor, instruction coalescing, performance

15 Code compression: Compiler optimization and ordering effects on VLIW code compression

Montserrat Ros, Peter Sutton

October 2003 **Proceedings of the 2003 international conference on Compilers, architecture and synthesis for embedded systems CASES '03**

Publisher: ACM Press

Full text available: pdf(334.18 KB) Additional Information: full citation, abstract, references, citings, index terms

Code size has always been an important issue for all embedded applications as well as larger systems. Code compression techniques have been devised as a way of battling bloated code; however, the impact of VLIW compiler methods and outputs on these compression schemes has not been thoroughly investigated.This paper describes the application of single- and multiple-instruction dictionary methods for code compression to decrease overall code size for the TI TMS320C6xxx DSP family. The compression ...

Keywords: VLIW, code compression, compiler optimizations

16 Dynamic coalescing for 16-bit instructions

Arvind Krishnaswamy, Rajiv Gupta

February 2005 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 4 Issue 1

Publisher: ACM Press

Full text available: pdf(487.89 KB) Additional Information: full citation, abstract, references, citings, index terms

In the embedded domain, memory usage and energy consumption are critical constraints.Embedded processors such as the ARM and MIPS provide a 16-bit instruction set, (called Thumb in the case of the ARM family of processors), in addition to the 32-bit instruction set to address these concerns. Using 16-bit instructions one can achieve code size reduction and instruction cache energy savings at the cost of performance. This paper

presents a novel approach that enhances the performance of 16-bit Thu ...

Keywords: 16-bit Thumb ISA, 32-bit ARM ISA, AX instructions, Embedded processor, code size, energy, instruction coalescing, performance

17 Code generation for compiled bit-true simulation for DSP application
L. De Coster, M. Adé, R. Lauwereins, J. Peperstaraete
December 1998 **Proceedings of the 11th international symposium on System synthesis ISSS '98**
Publisher: IEEE Computer Society
Full text available: pdf(1.13 MB) Additional Information: full citation, references, citings, index terms
Publisher Site

18 Standards: Proposed american standard: perforated tape code for information interchange
June 1964 **Communications of the ACM**, Volume 7 Issue 6
Publisher: ACM Press
Full text available: pdf(376.46 KB) Additional Information: full citation

19 Multiattribute hashing using Gray codes
Christos Faloutsos
June 1986 **ACM SIGMOD Record , Proceedings of the 1986 ACM SIGMOD international conference on Management of data SIGMOD '86**, Volume 15 Issue 2
Publisher: ACM Press
Full text available: pdf(883.73 KB) Additional Information: full citation, abstract, references, citings, index terms

Multiattribute hashing and its variations have been proposed for partial match and range queries in the past. The main idea is that each record yields a bitstring @@@@ ("record signature"), according to the values of its attributes. The binary value (@@@@)2 of this string decides the bucket that the record is stored. In this paper we propose to use Gray codes instead of binary codes, in order to map record signatures to buckets. In Gray codes, successive cod ...

20 Fast software implementation of error detection codes
David C. Feldmeier
December 1995 **IEEE/ACM Transactions on Networking (TON)**, Volume 3 Issue 6
Publisher: IEEE Press
Full text available: pdf(1.25 MB) Additional Information: full citation, references, citings, index terms

Terms used **hadamard order bit** Found **33,607** of **198,617**

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1 Track 14: quantum computing: Improving quantum circuit dependability with reconfigurable quantum gate arrays
Mihai Udrescu, Lucian Prodan, Mircea VI□duţiu
May 2005 **Proceedings of the 2nd conference on Computing frontiers CF '05**
Publisher: ACM Press
Full text available: pdf(343.73 KB) Additional Information: full citation, abstract, references, citings, index terms

The need for error detection and correction techniques is vital in quantum computation, due to the omnipresent nature of quantum errors. No realistic prospect of an operational quantum computational device may be warranted without such mechanisms. Therefore, the fact that error detecting and correcting techniques have been developed has enhanced the feasibility of a potential quantum computer [15] [18]. This paper presents a methodology for improving the fault tolerance of quantum circuits by us ...

Keywords: accuracy threshold, coding, reconfigurable quantum gate arrays

2 Signature of symmetric rational matrices and the unitary dual of lie groups
Jeffrey Adams, B. David Saunders, Zhendong Wan
July 2005 **Proceedings of the 2005 international symposium on Symbolic and algebraic computation ISSAC '05**
Publisher: ACM Press
Full text available: pdf(215.88 KB) Additional Information: full citation, abstract, references, index terms

A key step in the computation of the unitary dual of a Lie group is the determination if certain rational symmetric matrices are positive semi-definite. The size of some of the computations dictates that high performance integer matrix computations be used. We explore the feasibility of this approach by developing three algorithms for integer symmetric matrix signature and studying their performance both asymptotically and experimentally on a particular matrix family constructed from the excepti ...

Keywords: lie group, matrix signature, symmetric matrix

3 Session 3A: Exponential lower bound for 2-query locally decodable codes via a quantum argument
Iordanis Kerenidis, Ronald de Wolf

June 2003 **Proceedings of the thirty-fifth annual ACM symposium on Theory of computing STOC '03**
Publisher: ACM Press
Full text available: pdf(313.57 KB) Additional Information: full citation, abstract, references, citings, index terms

A locally decodable code encodes n-bit strings x in m-bit codewords $C(x)$, in such a way that one can recover any bit x_i from a corrupted codeword by querying only a few bits of that word. We use a *quantum* argument to prove that LDCs with 2 classical queries need exponential length: $m=2^{\Omega(n)}$. Previously this was known only for linear codes (Goldreich et al. 02). Our proof shows that a 2-query LDC can be decoded with only 1 ...

Keywords: locally decodable codes, private information retrieval, quantum computing

4 Session 9A: Generic quantum Fourier transforms
Cristopher Moore, Daniel Rockmore, Alexander Russell
January 2004 **Proceedings of the fifteenth annual ACM-SIAM symposium on Discrete algorithms SODA '04**
Publisher: Society for Industrial and Applied Mathematics
Full text available: pdf(170.02 KB) Additional Information: full citation, abstract, references, citings

The *quantum Fourier transform* (QFT) is the principal ingredient of most efficient quantum algorithms. We present a generic framework for the construction of efficient quantum circuits for the QFT by "quantizing" the highly successful *separation of variables* technique for the construction of efficient classical Fourier transforms. Specifically, we use Bratteli diagrams, Gel'fand-Tsetlin bases, and strong generating sets of small adapted diameter to provide efficient quantum circuits ...

5 Generic quantum Fourier transforms
Cristopher Moore, Daniel Rockmore, Alexander Russell
October 2006 **ACM Transactions on Algorithms (TALG)**, Volume 2 Issue 4
Publisher: ACM Press
Full text available: pdf(169.41 KB) Additional Information: full citation, abstract, references, index terms

The *quantum Fourier transform* (QFT) is a principal ingredient appearing in many efficient quantum algorithms. We present a generic framework for the construction of efficient quantum circuits for the QFT by "quantizing" the highly successful *separation of variables* technique for the construction of efficient classical Fourier transforms. Specifically, we apply Bratteli diagrams, Gel'fand-Tsetlin bases, and strong generating sets of small adapted diameter to provide effi ...

Keywords: Quantum computation, group theory

6 Multiple-transform pipelines for image coding
A. Antola
June 1988 **Proceedings of the 2nd international conference on Supercomputing ICS '88**
Publisher: ACM Press
Full text available: pdf(720.79 KB) Additional Information: full citation, abstract, references, index terms

Pipelined VLSI/WSI architectures supporting image coding transforms are defined and evaluated in the paper. The structures proposed in the paper have been derived by considering a common algorithmic kernel of the set of examined transforms. The possibility of reducing the computations to a common algorithmic version allows definition of flexible structures characterized by a "basic" pipeline - performing the common kernel

of computation - and by transform-dependent input and out ...

7 An introduction to quantum computing for non-physicists

September 2000 **ACM Computing Surveys (CSUR)**, Volume 32 Issue 3

Publisher: ACM Press

Full text available: pdf(491.89 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Richard Feynman's observation that certain quantum mechanical effects cannot be simulated efficiently on a computer led to speculation that computation in general could be done more efficiently if it used these quantum effects. This speculation proved justified when Peter Shor described a polynomial time quantum algorithm for factoring intergers.In quantum systems, the computational space increases exponentially with the size of the system, which enables exponential parallelism. ...

Keywords: complexity, parallelism, quantum computing

8 Special session on reliable computing: A dependability perspective on emerging technologies

Lucian Prodan, Mihai Udrescu, Mircea Vladutiu

May 2006 **Proceedings of the 3rd conference on Computing frontiers CF '06**

Publisher: ACM Press

Full text available: pdf(660.67 KB) Additional Information: full citation, abstract, references, index terms

Emerging technologies are set to provide further provisions for computing in times when the limits of current technology of microelectronics become an ever closer presence. A technology roadmap document lists biologically-inspired computing and quantum computing as two emerging technology vectors for novel computing architectures [43]. But the potential benefits that will come from entering the nanoelectronics era and from exploring novel nanotechnologies are foreseen to come at the cost of incr ...

Keywords: bio-inspired computing, bio-inspired digital design, dependability, embryonics, emerging technologies, evolvable hardware, fault-tolerance assessment, quantum computing, reliability

9 Shake 'em, but don't crack 'em: Cracking the Bluetooth PIN

Yaniv Shaked, Avishai Wool

June 2005 **Proceedings of the 3rd international conference on Mobile systems, applications, and services MobiSys '05**

Publisher: ACM Press

Full text available: pdf(223.67 KB) Additional Information: full citation, abstract, references

This paper describes the implementation of an attack on the Bluetooth security mechanism. Specifically, we describe a passive attack, in which an attacker can find the PIN used during the pairing process. We then describe the cracking speed we can achieve through three optimizations methods. Our fastest optimization employs an algebraic representation of a central cryptographic primitive (SAFER+) used in Bluetooth. Our results show that a 4-digit PIN can be cracked in less than 0.3 sec on an old ...

10 Quantum computing: Quantum designer and network simulator

Sándor Imre, Péter Abronits, Dániel Darabos

April 2004 **Proceedings of the 1st conference on Computing frontiers CF '04**

Publisher: ACM Press

Full text available: pdf(771.18 KB) Additional Information: full citation, abstract, references, index terms

In this paper we introduce our new quantum circuit design tool. Based on quantum mechanical models a universal discrete-time quantum-network designer and simulator was implemented. The graphical user interface allows the user to design complex quantum networks efficiently. The component-based architecture enables independent researchers to use our simulator API (written in C), while we continue to expand and refine the C# based user interface. Future plans include components for distributed simu ...

Keywords: quantum algorithms and circuits, quantum computing, simulation

11 Datapath and control for quantum wires

Nemanja Isailovic, Mark Whitney, Yatish Patel, John Kubiatowicz, Dean Copsey, Frederic T. Chong, Isaac L. Chuang, Mark Oskin

March 2004 **ACM Transactions on Architecture and Code Optimization (TACO)**, Volume 1 Issue 1

Publisher: ACM Press

Full text available: pdf(476.83 KB) Additional Information: full citation, abstract, references, citings, index terms

As quantum computing moves closer to reality the need for basic architectural studies becomes more pressing. Quantum wires, which transport quantum data, will be a fundamental component in all anticipated silicon quantum architectures. Since they cannot consist of a stream of electrons, as in the classical case, quantum wires must fundamentally be designed differently. In this paper, we present two quantum wire designs: a swap wire, based on swapping of adjacent qubits, and a teleportation wire, ...

Keywords: Architecture, Control, Layout

12 Locally testable codes and PCPs of almost-linear length

Oded Goldreich, Madhu Sudan

July 2006 **Journal of the ACM (JACM)**, Volume 53 Issue 4

Publisher: ACM Press

Full text available: pdf(749.48 KB) Additional Information: full citation, abstract, references, index terms

We initiate a systematic study of locally testable codes; that is, error-correcting codes that admit very efficient membership tests. Specifically, these are codes accompanied with tests that make a constant number of (random) queries into any given word and reject non-codewords with probability proportional to their distance from the code.Locally testable codes are believed to be the combinatorial core of PCPs. However, the relation is less immediate than commonly believed. Nevertheless, we sho ...

Keywords: Proof verification, derandomization, error-correcting codes, probabilistically checkable proofs

13 Networks I: The effect of communication costs in solid-state quantum computing architectures

Dean Copsey, Mark Oskin, Tzvetan Metodiev, Frederic T. Chong, Isaac Chuang, John Kubiatowicz

June 2003 **Proceedings of the fifteenth annual ACM symposium on Parallel algorithms and architectures SPAA '03**

Publisher: ACM Press

Full text available: pdf(149.00 KB) Additional Information: full citation, abstract, references, citings, index terms

Quantum computation has become an intriguing technology with which to attack difficult problems and to enhance system security. Quantum algorithms, however, have been analyzed under idealized assumptions without important physical constraints in mind. In this paper, we analyze two key constraints: the short spatial distance of quantum interactions and the short temporal life of quantum data.In particular, quantum computations must make use of extremely robust error correction techniques to exten ...

Keywords: quantum architecture, quantum computing, silicon-based quantum computing

14 Two-timescale simultaneous perturbation stochastic approximation using deterministic perturbation sequences

Shalabh Bhatnagar, Michael C. Fu, Steven I. Marcus, I-Jeng Wang

April 2003 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 13 Issue 2

Publisher: ACM Press

Full text available: pdf(294.83 KB) Additional Information: full citation, abstract, references, citings, index terms

Simultaneous perturbation stochastic approximation (SPSA) algorithms have been found to be very effective for high-dimensional simulation optimization problems. The main idea is to estimate the gradient using simulation output performance measures at only *two* settings of the *N*-dimensional parameter vector being optimized rather than at the $N + 1$ or $2N$ settings required by the usual one-sided or symmetric difference estimates, respectively. The two settings of the para ...

Keywords: Hadamard matrices, SPSA, Simulation optimization, deterministic perturbations, stochastic approximation, two-timescale algorithms

15 Symbolic simulation and verification: Gate-level simulation of quantum circuits

George F. Viamontes, Manoj Rajagopalan, Igor L. Markov, John P. Hayes

January 2003 **Proceedings of the 2003 conference on Asia South Pacific design automation ASPDAC**

Publisher: ACM Press

Full text available: pdf(114.53 KB) Additional Information: full citation, abstract, references, citings

Simulating quantum computation on a classical computer is a difficult problem. The matrices representing quantum gates, and vectors modeling qubit states grow exponentially with an increase in the number of qubits. However, by using a new data structure called the Quantum Information Decision Diagram (QuIDD) that exploits the structure of quantum operators, many of these matrices and vectors can be represented in a form that grows polynomially. Using QuIDDs, we implemented a general-purpose quan ...

16 Approximating the domatic number

Uriel Feige, Magnús M. Halldórsson, Guy Kortsarz

May 2000 **Proceedings of the thirty-second annual ACM symposium on Theory of computing STOC '00**

Publisher: ACM Press

Full text available: pdf(1.10 MB) Additional Information: full citation, references, citings, index terms

17 The APL theory of human vision

Gérard A. Langlet

August 1994 **ACM SIGAPL APL Quote Quad , Proceedings of the international conference on APL : the language and its applications: the language and its applications APL '94**, Volume 25 Issue 1
Publisher: ACM Press
Full text available: pdf(1.89 MB) Additional Information: full citation, references, citings, index terms, review

18 Poster session: FPGA implementation of a fast Hadamard transformer for WCDMA
Sanat Kamal Bahl, Jim Plusquellic
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays FPGA '03**
Publisher: ACM Press
Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

In code division multiple access (CDMA) systems the base station identifies each user in a cell by unique orthogonal (Walsh) codes. The Walsh codes are generated at the transmitter using a Walsh-Hadamard function. A Fast Hadamard Transformer (FHT) is used at the receiver to decode the transmitted codes. The purpose of this study is to design a FHT which utilizes less hardware resources as compared to the existing designs and also suggest means for reducing the input length of the Walsh sequence. ...

19 Concurrent error detection of fault-based side-channel cryptanalysis of 128-bit symmetric block ciphers
Ramesh Karri, Kaijie Wu, Piyush Mishra, Yongkook Kim
June 2001 **Proceedings of the 38th conference on Design automation DAC '01**
Publisher: ACM Press
Full text available: pdf(260.32 KB) Additional Information: full citation, abstract, references, index terms

Fault-based side channel cryptanalysis is very effective against symmetric and asymmetric encryption algorithms. Although straightforward hardware and time redundancy based concurrent error detection (CED) architectures can be used to thwart such attacks, they entail significant overhead (either area or performance). In this paper we investigate systematic approaches to low-cost, low-latency CED for symmetric encryption algorithms based on the inverse relationship that exists between encryp ...

20 MPEG: a video compression standard for multimedia applications
Didier Le Gall
April 1991 **Communications of the ACM**, Volume 34 Issue 4
Publisher: ACM Press
Full text available: pdf(9.16 MB) Additional Information: full citation, references, citings, index terms, review

Terms used **ovsf generate bit reorder** Found **39,110** of **198,617**

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1 Reconfigurable Signal Processing in Wireless Terminals

Jurgen Helmschmidt, Eberhard Schuler, Prashant Rao, Sergio Rossi, Serge di Matteo, Rainer Bonitz

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe: Designers' Forum - Volume 2 DATE '03**

Publisher: IEEE Computer Society

Full text available: pdf(399.68 KB) Publisher Site Additional Information: full citation, abstract, citings, index terms

In this paper, we show the necessity of reconfigurable hardware for data and signal processing in wireless mobile terminals. We first identify the key processing power requirements for realizing a third generation wireless mobile terminal with multi-link and multi-standard capabilities. This is done on the basis of two world applications: a flexible mobile rake receiver for UMTS/W-CDMA and an OFDM decoder for high-speed wireless LAN protocols. We present a software-defined concept and a system i ...

2 Circuit techniques for scaled technologies: A two-port SRAM for real-time video processor saving 53% of bitline power with majority logic and data-bit reordering

Hidehiro Fujiwara, Koji Nii, Junichi Miyakoshi, Yuichiro Murachi, Yasuhiro Morita, Hiroshi Kawaguchi, Masahiko Yoshimoto

October 2006 **Proceedings of the 2006 international symposium on Low power electronics and design ISLPED '06**

Publisher: ACM Press

Full text available: pdf(382.04 KB) Additional Information: full citation, abstract, references, index terms

We propose a low-power two-port SRAM suitable for real-time video processing. In order to minimize discharge power on a read bitline, a majority-logic decides if input data are inverted in a write cycle, so that "1"s are in the majority. In video data, since more significant bits of adjacent pixel data are fortunately lopsided to either "0" or "1" with higher probability, the data bits in the pixels are reordered in each digit group to exploit the majority logic. The speed and area overheads are ...

Keywords: data-bit reordering, low power SRAM, majority logic, real-time image processing, two-port SRAM

3 Generation of permutations for SIMD processors

Alexei Kudriavtsev, Peter Kogge

June 2005 **ACM SIGPLAN Notices , Proceedings of the 2005 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools for embedded systems LCTES '05**, Volume 40 Issue 7
Publisher: ACM Press

Full text available: pdf(356.05 KB) Additional Information: full citation, abstract, references, citings, index terms

Short vector (SIMD) instructions are useful in signal processing, multimedia, and scientific applications. They offer higher performance, lower energy consumption, and better resource utilization. However, compilers still do not have good support for SIMD instructions, and often the code has to be written manually in assembly language or using compiler builtin functions. Also, in some applications, higher parallelism could be achieved if compilers inserted permutation instructions that reorder t ...

Keywords: SIMD, permutations

4 Implicit array bounds checking on 64-bit architectures

Chris Bentley, Scott A. Watterson, David K. Lowenthal, Barry Rountree
December 2006 **ACM Transactions on Architecture and Code Optimization (TACO)**, Volume 3 Issue 4
Publisher: ACM Press

Full text available: pdf(548.20 KB) Additional Information: full citation, abstract, references, index terms

Several programming languages guarantee that array subscripts are checked to ensure they are within the bounds of the array. While this guarantee improves the correctness and security of array-based code, it adds overhead to array references. This has been an obstacle to using higher-level languages, such as Java, for high-performance parallel computing, where the language specification requires that all array accesses must be checked to ensure they are within bounds. This is because, in practic ...

Keywords: 64-bit architectures, Array-bounds checking, virtual memory

5 Caching I: New results on web caching with request reordering

Susanne Albers
June 2004 **Proceedings of the sixteenth annual ACM symposium on Parallelism in algorithms and architectures SPAA '04**
Publisher: ACM Press

Full text available: pdf(186.52 KB) Additional Information: full citation, abstract, references, index terms

We study web caching with request reordering. The goal is to maintain a cache of web documents so that a sequence of requests can be served at low cost. To improve cache hit rates, a limited reordering of requests is allowed. Feder et al. [6], who recently introduced this problem, considered caches of size 1, i.e. a cache can store one document. They presented an offline algorithm based on dynamic programming as well as online algorithms that achieve constant factor competitive ratios. For arbit ...

Keywords: approximation, batch, cache, competitive, document, offline, online

6 Using Rewriting Rules and Positive Equality to Formally Verify Wide-Issue Out-of-Order Microprocessors with a Reorder Buffer

M. Velev
March 2002 **Proceedings of the conference on Design, automation and test in Europe DATE '02**
Publisher: IEEE Computer Society

Full text available: pdf(192.83 KB) Additional Information: full citation, abstract, citings

Rewriting rules and Positive Equality [4] are combined in anautomatic way in order to formally verify out-of-order proces-sorsthat have a Reorder Buffer, and can issue/retire multipleinstructions per clock cycle. Only register-register instructionsare implemented, and can be executed out-of-order, as soon astheir data operands can be either read from the Register File, orforwarded as results of instructions ahead in program order inthe Reorder Buffer. The verification is based on the Burch andDi ...

7 Packet reordering is not pathological network behavior

Jon C. R. Bennett, Craig Partridge, Nicholas Shectman

December 1999 **IEEE/ACM Transactions on Networking (TON)**, Volume 7 Issue 6

Publisher: IEEE Press

Full text available: pdf(107.65 KB) Additional Information: full citation, references, citings, index terms

Keywords: Internet, communication system traffic, packet switching

8 W1-C: general symposium: New non-blocking EOVSF codes for multi-rate WCDMA system

Yih-Fuh Wang, Hsing-Hu Chen, Tun-Ying Lin

July 2006 **Proceeding of the 2006 international conference on Communications and mobile computing IWCMC '06**

Publisher: ACM Press

Full text available: pdf(886.94 KB) Additional Information: full citation, abstract, references, index terms

Orthogonal variable spreading factor (OVSF) codes are employed in the third generation (3G) wideband code division multiple access (WCDMA) wireless system as channelization codes. Any two codes OVSF of different levels are orthogonal if and only if one of two codes is not ancestor/descendant in each other. Therefore, when an OVSF code is assigned to a user, it blocks all of its ancestor and descendant codes. This results in a major drawback of OVSF codes, called blocking property: When an OVSF c ...

Keywords: EOVSF codes, OVSF codes, WCDMA, third generation (3G)

9 Scan-BIST based on cluster analysis and the encoding of repeating sequences

Lei Li, Zhanglei Wang, Krishnendu Chakrabarty

January 2007 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 12 Issue 1

Publisher: ACM Press

Full text available: pdf(523.07 KB) Additional Information: full citation, abstract, references, index terms

We present a built-in self-test (BIST) approach for full-scan designs that extracts the most frequently occurring sequences from deterministic test patterns. The extracted sequences are stored on-chip, and are used during test application. Three sets of test patterns are applied to the circuit under test during a BIST test session; these include pseudorandom patterns, semirandom patterns, and deterministic patterns. The semirandom patterns are generated based on the stored sequences and they are ...

Keywords: Built-in self-test (BIST), clustering test data volume, test compression

10 Code optimization - I: Optimization opportunities created by global data reordering

Gadi Haber, Moshe Klausner, Vadim Eisenberg, Bilha Mendelson, Maxim Gurevich

March 2003 **Proceedings of the international symposium on Code generation and optimization: feedback-directed and runtime optimization CGO '03**
Publisher: IEEE Computer Society

Full text available: pdf(1.31 MB) Additional Information: full citation, abstract, references, citings, index terms

Memory access has proven to be one of the bottlenecks in modern architectures. Improving memory locality and eliminating the amount of memory access can help release this bottleneck. We present a method for link-time profile-based optimization by reordering the global data of the program and modifying its code accordingly. The proposed optimization reorders the entire global data of the program, according to a representative execution rate of each instruction (or basic block) in the code. The da ...

11 WISQ: a restartable architecture using queues

A. R. Pleszkun, J. R. Goodman, W. C. Hsu, R. T. Joersz, G. Bier, P. Woest, P. B. Schechter
June 1987 **Proceedings of the 14th annual international symposium on Computer architecture ISCA '87**
Publisher: ACM Press

Full text available: pdf(1.14 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, the WISQ architecture is described. This architecture is designed to achieve high performance by exploiting new compiler technology and using a highly segmented pipeline. By having a highly segmented pipeline, a very-high-speed clock can be used. Since a highly segmented pipeline will require relatively long pipelines, a way must be provided to minimize the effects of pipeline bubbles that are formed due to data and control dependencies. It is also important to provide a way ...

12 Temperature and power aware architectures: Reducing reorder buffer complexity through selective operand caching

Gurhan Kucuk, Dmitry Ponomarev, Oguz Ergin, Kanad Ghose
August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design ISLPED '03**
Publisher: ACM Press

Full text available: pdf(80.27 KB) Additional Information: full citation, abstract, references, citings, index terms

Modern superscalar processors implement precise interrupts by using the Reorder Buffer (ROB). In some microarchitectures , such as the Intel P6, the ROB also serves as a repository for the uncommitted results. In these designs, the ROB is a complex multi-ported structure that dissipates a significant percentage of the overall chip power. Recently, a mechanism was introduced for reducing the ROB complexity and its power dissipation through the complete elimination of read ports for reading out so ...

Keywords: low-complexity datapath, low-power design, reorder buffer, short-lived values

13 Compilers: Implicit java array bounds checking on 64-bit architecture

Chris Bentley, Scott A. Watterson, David K. Lowenthal, Barry Rountree
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Publisher: ACM Press

Full text available: pdf(188.75 KB) Additional Information: full citation, abstract, references, index terms

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ensure they are within bounds. In practice, array bounds checking in scientific applications may increase execution time by more than a factor of 2. Previous research has explored optimizations to statically eliminate bounds checks, but the dy ...

Keywords: array-bounds checking, java, virtual memory

14 Co-synthesis of pipelined structures and instruction reordering constraints for instruction set processors

Ing-Jer Huang

January 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 1

Publisher: ACM Press

Full text available: pdf(1.58 MB) Additional Information: full citation, abstract, references, index terms

This paper presents a hardware/software co-synthesis approach to pipelined ISP (instruction set processor) design. The approach synthesizes the pipeline structure from a given instruction set architecture (behavioral) specification. In addition, it generates a set of reordering constraints that guides the compiler back-end (reorderer) to properly schedule instructions so that possible pipeline hazards are avoided and throughput is improved.Co-synthesis takes place while resolving ...

Keywords: compiler instruction optimization\, instruction set processor, pipeline hazards, pipeline taxonomy, synthesis

15 Testing: Two dimensional reordering of functional test data for compression by ATE

Hamidreza Hashempour, Fabrizio Lombardi

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Publisher: ACM Press

Full text available: pdf(121.41 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a novel approach for compressing functional test data in Automatic Test Equipment (ATE). A practical technique is presented for 2 Dimensional (2D) reordering of test data in which additionally to test vector reordering, column reordering is also applied. An ATE based approach to extract the original test vectors from the 2D ordered data is presented. The advantage of the approach is substantiated using the figure of merit of entropy for the 2D ordered test data of ISCAS bench ...

Keywords: 2D reordering, ATE, column reordering, functional test data, scan test data, test data compression

16 PL/I program efficiency

Michael McNeil, William Tracz

June 1980 **ACM SIGPLAN Notices**, Volume 15 Issue 6

Publisher: ACM Press

Full text available: pdf(1.29 MB) Additional Information: full citation, abstract, references, citings

All PL/I Programmers should be aware of and genuinely concerned about PL/I Program efficiency. This paper addresses the following question:"How do you write a PL/I program which the PL/I Complier will reduce to the smallest and fastest executing machine language module?" The real world payoffs of knowing how the PL/I Optizing Compiler handles different syntactical representations of similar semantic relationships with respect to code generation and storage allocation can increase program runtime ...

17 Re-Configurable Bus Encoding Scheme for Reducing Power Consumption of the Cross Coupling Capacitance for Deep Sub-Micron Instruction Bus
Siu-Kei Wong, Chi-Ying Tsui
February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 1 DATE '04**
Publisher: IEEE Computer Society
Full text available: pdf(152.05 KB) Additional Information: full citation, abstract, index terms

In very deep sub-micron designs, cross coupling capacitances become the dominant factor of the total bus loading and have a significant impact on the power consumption. In this paper, we propose two reconfigurable bus encoding schemes, which are based on the correlation among the bit lines, to reduce the power consumption at the cross coupling capacitances of the instruction buses. The instruction is encoded by flipping and reordering the bit lines during compilation time to reduce the total swi ...

18 Poster session 2: Orthogonal code generator for 3G wireless transceivers
Boris D. Andreev, Edward L. Titlebaum, Eby G. Friedman
April 2003 **Proceedings of the 13th ACM Great Lakes symposium on VLSI GLSVLSI '03**
Publisher: ACM Press
Full text available: pdf(152.16 KB) Additional Information: full citation, abstract, references, index terms

Orthogonal variable spreading factor (OVSF) codes are standard in third generation UMTS cellular systems. The efficient generation of these codes is essential for reducing the area and power of wireless transceivers. In this paper, the basic properties of this family of codes are analyzed from an RTL perspective and two efficient hardware code generators are proposed. Tradeoffs and design solutions as well as low power considerations are discussed. These results represent the first reported impl ...

Keywords: 3GPP, CDMA, OVSF codes, UMTS, VLSI, WCDMA

19 Fabric-driven logic synthesis: Layout-aware synthesis of arithmetic circuits
Junhyung Um, Taewhan Kim
June 2002 **Proceedings of the 39th conference on Design automation DAC '02**
Publisher: ACM Press
Full text available: pdf(127.44 KB) Additional Information: full citation, abstract, references, citings, index terms

In deep sub-micron (DSM) technology, wires are equally or more important than logic components since wire-related problems such as crosstalk, noise are much critical in system-on-chip (SoC) design. Recently, a method [12] for generating a partial product reduction tree (PPRT) with optimal-timing using bit-level adders to implement arithmetic circuits, which outperforms the current best designs, is proposed. However, in the conventional approaches including [12], interconnects are not primary com ...

Keywords: carry-save-adder, high performance, layout

20 Ad hoc networks: OVSF-CDMA code assignment in wireless ad hoc networks
Peng-Jun Wan, Xiang-Yang Li, Ophir Frieder
October 2004 **Proceedings of the 2004 joint workshop on Foundations of mobile computing DIALM-POMC '04**
Publisher: ACM Press
Full text available: pdf(198.79 KB) Additional Information: full citation, abstract, references, citings, index terms

Orthogonal Variable Spreading Factor (OVSF) CDMA code provides a means of support of

variable rate data service at low hardware cost. In contrast to the conventional orthogonal fixed-spreading-factor CDMA code, OVSF-CDMA code consists of an infinite number of codewords with variable rates but not every pair of codewords are orthogonal to each other. In an OVSF-CDMA wireless ad hoc network, a code assignment has to be conflict-free, i.e., two nodes can be assigned the same codeword or two non-ort ...

Keywords: OVSF-CDMA, approximation algorithms, code assignment, graph theory, system design

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

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Try this search in The ACM Guide

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Best 200 shown Relevance scale

1 Optimizing data permutations for SIMD devices
Gang Ren, Peng Wu, David Padua
June 2006 **ACM SIGPLAN Notices , Proceedings of the 2006 ACM SIGPLAN conference on Programming language design and implementation PLDI '06**, Volume 41 Issue 6
Publisher: ACM Press
Full text available: pdf(260.98 KB) Additional Information: full citation, abstract, references, citings, index terms

The widespread presence of SIMD devices in today's microprocessors has made compiler techniques for these devices tremendously important. One of the most important and difficult issues that must be addressed by these techniques is the generation of the data permutation instructions needed for non-contiguous and misaligned memory references. These instructions are expensive and, therefore, it is of crucial importance to minimize their number to improve performance and, in many cases, enable speed ...

Keywords: SIMD compilation, data permutation, optimization

2 Effective compiler generation by architecture description
Stefan Farfeleder, Andreas Krall, Edwin Steiner, Florian Brandner
June 2006 **ACM SIGPLAN Notices , Proceedings of the 2006 ACM SIGPLAN/SIGBED conference on Language, compilers and tool support for embedded systems LCTES '06**, Volume 41 Issue 7
Publisher: ACM Press
Full text available: pdf(128.18 KB) Additional Information: full citation, abstract, references, index terms

Embedded systems have an extremely short time to market and therefore require easily retargetable compilers. Architecture description languages (ADLs) provide a single concise architecture specification for the generation of hardware, instruction set simulators and compilers. In this article, we present an ADL for compiler generation. From a specification, we can derive an optimized tree pattern matching instruction selector, a register allocator and an instruction scheduler. Compared to a hand- ...

Keywords: architecture description language, code generation, compiler generation

3 Reversible logic circuit synthesis
Vivek V. Shende, Aditya K. Prasad, Igor L. Markov, John P. Hayes

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design ICCAD '02**
Publisher: ACM Press
Full text available: pdf(246.56 KB) Additional Information: full citation, abstract, references, citings, index terms

Reversible or information-lossless circuits have applications in digital signal processing, communication, computer graphics and cryptography. They are also a fundamental requirement in the emerging field of quantum computation. We investigate the synthesis of reversible circuits that employ a minimum number of gates and contain no redundant input-output line-pairs (temporary storage channels). We prove constructively that every even permutation can be implemented without temporary storage using ...

4 Advances in synthesis: Transformation rules for designing CNOT-based quantum circuits
Kazuo Iwama, Yahiko Kambayashi, Shigeru Yamashita
June 2002 **Proceedings of the 39th conference on Design automation DAC '02**
Publisher: ACM Press
Full text available: pdf(283.51 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper gives a simple but nontrivial set of local transformation rules for *Control-NOT (CNOT)*-based combinatorial circuits. It is shown that this rule set is complete, namely, for any two equivalent circuits, S1 and S2, there is a sequence of transformations, each of them in the rule set, which changes S1 to S2. Our motivation is to use this rule set for developing a design theory for *quantum circuits* whose Boolean logic parts should b ...

Keywords: CNOT gate, local transformation rules, quantum circuit

5 Symbolic simulation and verification: Gate-level simulation of quantum circuits
George F. Viamontes, Manoj Rajagopalan, Igor L. Markov, John P. Hayes
January 2003 **Proceedings of the 2003 conference on Asia South Pacific design automation ASPDAC**
Publisher: ACM Press
Full text available: pdf(114.53 KB) Additional Information: full citation, abstract, references, citings

Simulating quantum computation on a classical computer is a difficult problem. The matrices representing quantum gates, and vectors modeling qubit states grow exponentially with an increase in the number of qubits. However, by using a new data structure called the Quantum Information Decision Diagram (QuIDD) that exploits the structure of quantum operators, many of these matrices and vectors can be represented in a form that grows polynomially. Using QuIDDs, we implemented a general-purpose quan ...

6 Systems session 3: assorted topics: Very low complexity MPEG-2 to H.264 transcoding using machine learning
Gerardo Fernández, Pedro Cuenca, Luis Orozco Barbosa, Hari Kalva
October 2006 **Proceedings of the 14th annual ACM international conference on Multimedia MULTIMEDIA '06**
Publisher: ACM Press
Full text available: pdf(1.33 MB) Additional Information: full citation, abstract, references, index terms

This paper presents a novel macroblock mode decision algorithm for inter-frame prediction based on machine learning techniques to be used as part of a very low complexity MPEG-2 to H.264 video transcoder. Since coding mode decisions take up the most resources in video transcoding, a fast macro block (MB) mode estimation would lead

to reduced complexity. The proposed approach is based on the hypothesis that MB coding mode decisions in H.264 video have a correlation with the distribution of the mo ...

Keywords: H.264, MPEG-2, inter-frame, machine learning, transcoding

7 Poster Session 2: Odd/even bus invert with two-phase transfer for buses with coupling

Yan Zhang, John Lach, Kevin Skadron, Mircea R. Stan

August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design ISLPED '02**

Publisher: ACM Press

Full text available: pdf(239.83 KB) Additional Information: full citation, abstract, references, citings, index terms

The coupling capacitances between on-chip bus lines become dominant in deep-submicron technologies. Coding to reduce the *switching activity* of the individual lines was enough to reduce power on buses in older technologies, but new coding techniques that reduce the *coupling activity* between lines are needed for deep-submicron buses. One such coding technique uses the simple observation that coupling capacitances are always charged and discharged by activity on neighboring bus lines, ...

Keywords: bus invert, buses with coupling, coding for low-power I/O

8 Circuit techniques for scaled technologies: A two-port SRAM for real-time video processor saving 53% of bitline power with majority logic and data-bit reordering

Hidehiro Fujiwara, Koji Nii, Junichi Miyakoshi, Yuichiro Murachi, Yasuhiro Morita, Hiroshi Kawaguchi, Masahiko Yoshimoto

October 2006 **Proceedings of the 2006 international symposium on Low power electronics and design ISLPED '06**

Publisher: ACM Press

Full text available: pdf(382.04 KB) Additional Information: full citation, abstract, references, index terms

We propose a low-power two-port SRAM suitable for real-time video processing. In order to minimize discharge power on a read bitline, a majority-logic decides if input data are inverted in a write cycle, so that "1"s are in the majority. In video data, since more significant bits of adjacent pixel data are fortunately lopsided to either "0" or "1" with higher probability, the data bits in the pixels are reordered in each digit group to exploit the majority logic. The speed and area overheads are ...

Keywords: data-bit reordering, low power SRAM, majority logic, real-time image processing, two-port SRAM

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Alexei Kudriavtsev, Peter Kogge

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Gurhan Kucuk, Dmitry Ponomarev, Oguz Ergin, Kanad Ghose
August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design ISLPED '03**
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Keywords: 2D reordering, ATE, column reordering, functional test data, scan test data, test data compression

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Results for "((ovsf code)<in>metadata)"
Your search matched **92** of **1516137** documents.
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IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

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Web Results **1** - **10** of about **35** for **ovsf code, generate, bit reorder**. (**0.25** seconds)

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OVSF Code Generator, **Generate** orthogonal variable spreading factor (**OVSF**) **code** ...
Algebraic Interleaver, **Reorder** input symbols using algebraically derived ...
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OVSF Code Generator, **Generate** orthogonal variable spreading factor (**OVSF**) **code** from set of ... General Block Interleaver, **Reorder** symbols in input vector ...
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SYSTEM FOR GENERATING PSEUDORANDOM SEQUENCES - Patent EP1386462
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Programmable digital signal processor including a clustered SIMD ...
A configurable block interleaver accelerator may be used to **reorder** data to spread ... a de-scrambling **code generator** or from an **OVSF code generator**. ...
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Each branch is spread with a 128 Walsh **code** to **generate** a SR. of 1.2288 Mcps. In this case, ... **Bit**-reverse (**OVSF codes**). Actual **code Code** number ...
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arrive out of order the destination node needs to **reorder** the packets ... a **code**. The **code** is a pseudo-random sequence of ±1, where the **bit** rate of the **code** ...
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[PDF] Designing and Testing cdma2000 Base Stations
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OVSF codes and Walsh **codes** are the same, only their **code** number. assignment is different. The generation method is called "**bit**-reverse" ...
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The reordering buffers in Figure 12.6 are used to **reorder** the data of different ... **OVSF code** exhaustion: every additional pilot channel requires an ...
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The channelization **codes** are Orthogonal Variable Spreading Factor (**OVSF**) **codes** defined by ... Instead the encoder needs to **generate** a scalable **bit**- ...
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Hadamard Code Generator, **Generate Hadamard code** from orthogonal set of **codes** ...
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SYSTEM FOR GENERATING PSEUDORANDOM SEQUENCES - Patent EP1386462
The **code generator** of claim 2 further comprising **bit** reordering means, ... [0037] An example of generating a **Hadamard code** will be explained with reference ...
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Non-recursively generated orthogonal PN **codes** for variable rate ...
reordering columns of the **Hadamard** matrix in accordance with a reordering **code** to **generate** a reordered **Hadamard** matrix; and ...
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8 illustrates the generation of the forth **code** of the **Hadamard code** tree having a ... The **code generator** of claim 2 further comprising **bit** reordering means, ...
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[Paper] Implementation Overview of a WCDMA Transceiver on an FPGA ...
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[PDF] Optimal measurement techniques utilizing **Hadamard** transforms ...
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Recall that in the simplex-**code** decomposition the **generator**. matrix G contains n columns representing every possible m-. **bit** sequence except the zero ...
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of the **code generator** matrices, one for each antenna, has to be ... binary **Hadamard** sequences with length four. Each **code** block ...
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Multiple access communications system and method using **code** and ...
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8 illustrates one suitable embodiment of the PN **code generator** 20 for a ... Reordered

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Walsh Code Generator, **Generate Walsh code** from orthogonal set of **codes** ... Algebraic Interleaver, **Reorder** input symbols using algebraically derived ...
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A METHOD OF QUADRATURE SPREADING - Patent EP1350335
[0012] Following **Walsh** spreading, all **code** channels undergo Quadrature Spreading, ... The Long **Code Generator** produces long **codes**, which are 42 **bit** ...
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The pilot channel is always spread with **Walsh code** 0, the SYNC channel is always spread ... The Long **Code Generator** produces long **codes**, which are 42 **bit** ...
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correctly **reorder** the convolution values to return back to ... An 8-point **Walsh** transform is used for the. 7. **bit**-length PN. **code**. After omitting the first ...
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multipath. fading. channel. PN. sequence. **generator** and. 4. **Walsh code** ... used to **reorder** the data back to their ori,$nal sequence. After ...
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code domain channels is to **reorder**. them so related **code** channels are. displayed adjacent to each other. The **bit**-reversed generation of. **Walsh** channels ...
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Each branch is spread with a 128 **Walsh code** to **generate** a SR. of 1.2288 Mcps. In this case, ... If a high data rate channel using a 4-**bit Walsh code** such as ...
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Non-recursively generated orthogonal PN **codes** for variable rate ...
8 illustrates one suitable embodiment of the PN **code generator** 20 for a ... Note that one could also **reorder** by moving column 1 (of the **Walsh code**) to 3, ...

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a **reorder** unit coupled to the encoder to **generate** coded data as a **code** ... The encoding system defined in claim 22 wherein the **bit generator codes** data ...
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